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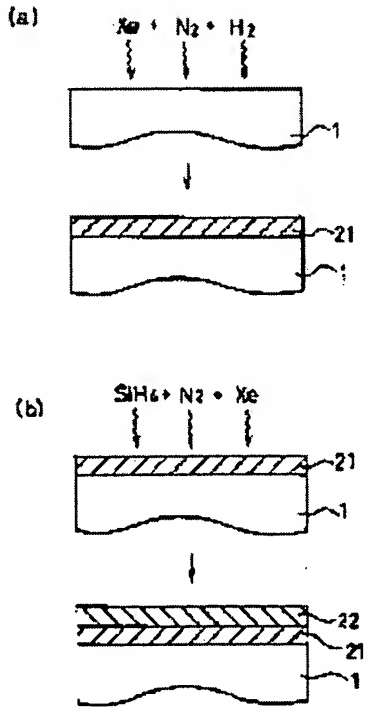
(54) MANUFACTURE OF SEMICONDUCTOR AND MANUFACTURING APPARATUS OF SEMICONDUCTOR

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a method and apparatus for manufacturing a semiconductor for smoothly operating film quality control on a boundary face between a silicon substrate and an SiN film, and for forming the SiN film with high quality in a short time.

SOLUTION: A wafer made of silicon as main components is irradiated with microwaves via a planar antenna member RLSA 60, having plural slits under a treating gas atmosphere so that plasma containing oxygen, or nitride, or oxygen and nitride can be formed, and oxidation, or nitriding, or oxidation/ nitriding is carried out directly to the surface of the wafer by using this plasma, and an insulating film 21 which is 1 nm or less in film thickness converted equivalent to film thickness of an oxide film.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of a semiconductor, and relates to a detail further at the gate-dielectric-film formation approach in an MIS mold semiconductor device.
[0002]
[Description of the Prior Art] Recently, very thin gate dielectric film about 4nm or less is demanded with detailed-izing of an MIS mold semiconductor device. Conventionally, the silicon oxide (SiO2 film) obtained by direct oxidation of a silicon substrate, using about C 850-degree C-1000-degree furnace [heating-at-high-temperature] as a gate-dielectric-film ingredient has been used industrially.
[0003] However, SiO2 If the film is made thin to 4nm or less, the leakage current (gate leakage current) which flows this gate dielectric film will increase, and problems, such as increase of power consumption and acceleration of device property degradation, will arise.
[0004] Moreover, the boron contained at the gate concerned at the time of gate electrode formation is SiO2. It runs through the film, a silicon substrate is reached, and the problem of degrading a semiconductor device property is also produced. As one approach of solving such a trouble, the nitride (SiN film) is examined as a gate-dielectric-film ingredient.
[0005] If this SiN film is formed with a CVD method, much imperfect association (dangling bond) will occur in an interface with a silicon substrate, and a device property will deteriorate. Therefore, by the SiN film formation concerned, it is thought that the approach of nitriding directly the silicon substrate which used the plasma is promising. The reason for nitriding directly is for obtaining the gate dielectric film of high quality with little interface state density.
[0006] Moreover, the reason using the plasma is for forming the SiN film at low temperature. If the SiN film is nitrided with heating, the elevated temperature more than 1000-degreeC is required, and when the dopant injected into the silicon substrate like this heat process carries out difference diffusion, a device property will deteriorate. Such an approach is indicated by JP,55-134937,A, JP,59-4059,A, etc.
[0007] However, since it is accelerated with plasma sheath potential and incidence of the ion in the plasma is carried out to a silicon substrate with high energy when forming the SiN film using the plasma, the so-called plasma damage occurs in a silicon substrate interface or a silicon substrate, and the problem that a device property arises is pointed out.
[0008] To this problem, electron temperature is low and microwave plasma equipment equipped with the flat antenna which has the slit of a majority of small plasma damages is reported.
[0009] (p. Ultra Clean technology Vol.10 Supplement 1, 32, 1998, Published byUltra Clean Society) .
[0010] If this plasma equipment is used, a plasma damage can be sharply reduced to

the conventional plasma whose electron temperature is about 1eV or less and whose plasma sheath electrical potential difference is about 50V since a plasma sheath electrical potential difference also becomes several V less or equals.
[0011] However, in order to acquire a good interface with few joint defects by making oxygen unevenly distributed only in a silicon substrate interface in forming the SiN film by direct nitriding even when performing silicon nitriding treatment using this plasma equipment, there is a problem that the membraneous control by the interface with a silicon substrate is difficult.
[0012] Furthermore, in order that nitriding may progress when this plasma equipment is used, and a nitrogen atom is spread in a silicon substrate, there is a problem that a nitriding rate is slow, the time amount which performs predetermined processing to a processed object is long, there is little processing number of sheets of the processed object per unit time amount, and it cannot use industrially. For example, per throughput demanded from the point of mass-production manufacture, for example, a processed object, when forming the 4nm SiN film, even if it adjusts various plasma conditions, such as a pressure and microwave power, it takes about 5 minutes or more, and is much less than the desired value of the processing time of about 1 minute.
[0013]
[Problem(s) to be Solved by the Invention] This invention is made in order to solve the above-mentioned conventional trouble. Namely, this invention aims at offering the manufacture approach of a semi-conductor and manufacturing installation which can perform membraneous control by the interface of a silicon substrate and the SiN film with the sufficient result.
[0014] Moreover, this invention aims at offering the manufacture approach of a semi-conductor and manufacturing installation which can form the SiN film of high quality in a short time.
[0015]
[Means for Solving the Problem] For the above-mentioned purpose achievement, the semi-conductor manufacture approach of this invention By irradiating microwave under a raw gas ambient atmosphere through the flat antenna member which has two or more slits in the processed base which uses silicon as a principal component, oxygen, Or it is characterized by forming the plasma containing nitrogen or oxygen, and nitrogen, performing oxidation, nitriding, or acid nitriding to said processed base front face directly, and forming the insulator layer of thickness (silicon oxide conversion) 1nm or less in it using this plasma.
[0016] By the semi-conductor manufacture approach of this invention, since insulator layer thickness is 1nm or less, nitriding of a silicon substrate serves as the processes with the main process to which the nitrogen atom, oxygen atom or nitrogen atom generated by not diffusion but the plasma, and an oxygen atom react with a silicon substrate surface, and a short time for about 30 seconds can perform a nitriding rate.
[0017] Since the film production rate of 3 or more nm/min can attain comparatively easily when forming the remaining insulator layers with a CVD method on this direct nitriding or the thin film insulator layer which oxidized or nitrided [acid], the insulator layer of the thickness which is total 4nm can also be formed within 2 minutes.

[0018] Furthermore, by the semi-conductor manufacture approach of this invention, since the process which forms a good insulator layer in an interface with a silicon substrate by direct nitriding, oxidation, or acid nitriding, and the process which forms the remaining insulator layers with a CVD method on it can be performed independently, altogether, with direct nitriding or a CVD method, compared with the approach of forming an insulator layer, the membraneous controllability in a silicon substrate interface can improve, and a better insulator layer can be formed.
[0019] Setting to this semi-conductor manufacture approach, said raw gas is N2. Or N2 O, NO, or NH3 The included gas is mentioned. This raw gas may contain rare gas, such as an argon.

[0020] Other semi-conductor manufacture approaches of this invention silicon to moreover, the processed base used as a principal component under a raw gas ambient atmosphere By irradiating microwave through the flat antenna member which has two or more slits, oxygen, Or it is characterized by providing the process which forms the plasma containing nitrogen or oxygen, and nitrogen, performs oxidation, nitriding, or acid nitriding to said processed base front face directly, and forms the 1st insulator layer in it using this plasma, and the process which forms the 2nd insulator layer on said 1st insulator layer.
[0021] In the above-mentioned semi-conductor manufacture approach, the insulator layer which said 2nd insulator layer turns into from silicon nitride is mentioned.
[0022] The process which forms this 2nd insulator layer may be performed with a CVD method, and a plasma exposure may perform it.
[0023] Formation of this 2nd insulator layer is N2. Or NH3 And the approach of forming by supplying the plasma containing a mono silane, a dichloro silane, or trichlorosilan is mentioned.
[0024] Since according to the semi-conductor manufacture approach of this invention the direct plasma is supplied on a silicon substrate by the approach using the so-called RLSA (Radial Line Slot Antenna) antenna of irradiating microwave through the flat antenna member which has two or more slits and a SiN insulator layer is formed in the processed base which uses silicon as a principal component under a raw gas ambient atmosphere, membraneous control of the interface of a silicon substrate and the SiN insulator layer formed in the front face can be performed with the sufficient result.
[0025] Furthermore, according to other semi-conductor manufacture approaches of this invention, since the 1st insulator layer was formed upwards by the approach using the so-called RLSA antenna and the whole of the 2nd insulator layer is formed by low damage plasma exposure, the SiN film of high quality can be formed. When forming especially the 2nd insulator layer with a CVD method, film production in a short time is attained, and the SiN film of high quality can be formed in a short time.
[0026]
[Embodiment of the Invention] The gestalt of one operation of this invention is explained below.
[0027] About an example of the structure of the semiconductor device first manufactured by the semi-conductor manufacture approach of this invention, the semiconductor device equipped with gate dielectric film as an insulator layer is made into an example, and drawing 1 explains it.
[0028] As for a silicon substrate and 11, one in drawing is [field oxide and 2] gate dielectric film, and 13 is a gate electrode. It is formed in the 1st insulator layer 21 with a thickness of about 1nm and the top face of the 1st insulator layer 21 which consist of a high insulator layer of quality formed in the interface with a silicon substrate 1 as this GUTO insulator layer 2 is shown in drawing 1 (b) by this invention having the description in gate dielectric film 2, for example, is constituted by the 2nd film 22 with a thickness of about 3nm.
[0029] In this example, the 1st high film 21 of quality silicon to the processed base used as a principal component under a raw gas ambient atmosphere By irradiating microwave through the flat antenna member which has two or more slits, oxygen, Or it consists of the 1st silicon acid nitride (henceforth the "SiON film") which formed the plasma containing nitrogen or oxygen, and nitrogen, and was formed in said processed base front face by performing oxidation, nitriding, or acid nitriding directly using this plasma.
[0030] Moreover, the 2nd film 22 with a larger membrane formation rate than the 1st film 21 is formed of the process which forms the 2nd insulator layer on said 1st insulator layer.
[0031] Next, the formation approach of such gate dielectric film 2 is explained.
[0032] Drawing 2 is the schematic diagram showing the whole semiconductor-fabrication-machines-and-equipment 30 configuration for enforcing the semi-

conductor manufacture approach of this invention.
[0033] it is shown in drawing 2 -- as -- semiconductor fabrication machines and equipment 30 -- the conveyance room 31 is mostly arranged in the center, and the plasma treatment unit 32, the load lock units 34 and 35 of 33 or 2 CVD processing units, and the heating unit 36 are arranged so that the perimeter of this conveyance room 31 may be surrounded.
[0034] The reserve refrigeration unit 45 and the refrigeration unit 46 are arranged beside the load lock units 34 and 35, respectively.
[0035] The conveyance arms 37 and 38 are arranged in the interior of the conveyance room 31, and Wafer W is conveyed among said each units 32-36.
[0036] The loader arms 41 and 42 are arranged in the before [a drawing metacarpus] side of the load lock units 34 and 35. These loader arms 41 and 42 take Wafer W in and out among four sets of the cassettes 44 set on the cassette stage 43 further arranged in the near side.
[0037] In addition, the CVD processing unit 33 in drawing 2 is as exchangeable as the plasma treatment unit 32 and the plasma treatment unit of isomorphism, and may set two plasma treatment units.
[0038] Furthermore, both these plasma treatment unit 32 and the CVD processing unit 33 are as exchangeable as the single chamber mold plasma / CVD processing unit, and it is also possible to set one set or two sets of the single chamber mold plasma / CVD processing units to the location of the plasma treatment unit 32 or the CVD processing unit 33. They are [the approach of CVD(ing) the plasma SiN film in the processing unit 33 after forming the direct SiON film in the processing unit 32, when the number of plasma treatment is two, and] direct SiON film formation and SiN to juxtaposition at the processing units 32 and 33. CVD film formation may be performed. Or it is SiN with another equipment after performing direct SiON film formation to juxtaposition in the processing units 32 and 33. CVD film formation can also be performed.
[0039] Drawing 3 is the vertical cross section of the plasma treatment unit 32 used for membrane formation of gate ****** 2.
[0040] 50 is the vacuum housing formed of aluminum. The gas supply room 54 of the shape of a flat cylindrical shape constituted with dielectrics, such as nitriding aluminum, so that the substrate 51, for example, larger opening than Wafer W, might be formed in the top face of this vacuum housing 50 and this opening 51 might be plugged up is formed. Many gas supply holes 55 are formed in the inferior surface of tongue of this gas supply room 54, and the gas introduced into the gas supply room 54 is supplied in the shape of a shower in a vacuum housing 50 through the gas supply hole 55 concerned.
[0041] The waveguide 63 connected to the microwave power supply section 61 which generates nothing, for example, 2.45GHz microwave, in the RF power supply section is formed in the outside of the gas supply room 54 through the radial line slot antenna (it is hereafter written as "RLSA".) 60 formed by the copper plate. Flat circular-waveguide 63A by which, as for this waveguide 63, the margo inferior was connected to RLSA60, Cylindrical shape waveguide 63B by which the end side was connected to the top face of this circular-waveguide 63A, An end side is connected to a right angle on the side face of coaxial guided wave converter 63C ****(ed) by the top face of this cylindrical shape waveguide 63B, and this coaxial guided wave converter 63C, and it is constituted combining rectangular waveguide 63D by which the other end side was connected to the microwave power supply section 61.
[0042] By this invention, it is called the RF field here including UHF and microwave, and high-frequency power supplied by the RF power supply section shall be made into 300MHz or more a thing 2500MHz or less including UHF 300MHz [or more] or microwave 1GHz or more, and shall call the RF plasma the plasma generated by such high-frequency power. the end side of the shank 62 which turns into the interior of said said cylindrical shape ****** 63B from a conductive ingredient -- the top face of RLSA60 -- it is prepared in the shape of the same axle so that it may connect in the

center mostly and an other end side may connect with the top face of cylindrical shape waveguide 63B, and thereby, the waveguide 63B concerned is constituted as a coaxial waveguide.
[0043] The gas supply line 72 is formed in the location of 16 places equally arranged, for example along that hoop direction on the side attachment wall by the side of the upper part of a vacuum housing 50, and the gas which contains rare gas and N from this gas supply line 72 is supplied equally without nonuniformity near the plasma field P of a vacuum housing 50.
[0044] Moreover, in the vacuum housing 50, the installation base 52 of Wafer W is formed so that it may counter with the gas supply room 54. The temperature control part which is not illustrated is built in this installation base 52, and, thereby, the installation base 52 concerned functions as a hot platen. Furthermore the end side of an exhaust pipe 53 is connected to the pars basilaris ossis occipitalis of a vacuum housing 50, and the other end side of this exhaust pipe 53 is connected to the vacuum pump 55.
[0045] Drawing 4 is a top view of RLSA60 used for the semiconductor fabrication machines and equipment of this invention.
[0046] As shown in drawing 4 , in this RLSA60, two or more slots 60a and 60a and -- are formed in the front face concentric circular. Each slot 60a is the slot which the abbreviation rectangle penetrated, and adjoining slots are arranged so that it may intersect perpendicularly mutually and the alphabetic character of "T" of the abbreviation alphabet may be formed. The die length and array spacing of slot 60a are determined according to the wavelength of the microwave generated from the microwave power supply section 61. Drawing 5 is the vertical cross section having shown typically the CVD processing unit 33 used for the semiconductor fabrication machines and equipment of this invention.
[0047] As shown in drawing 5 , the processing room 82 of the CVD processing unit 33 is formed in the structure in which an airtight is possible of aluminum etc. Although omitted in drawing 5 , in the processing room 82, it has the heating device and the cooler style.
[0048] The gas installation tubing 83 which introduces gas in the center of the upper part is connected to the processing room 82, and the inside of the processing room 82 and the gas installation tubing 83 is opened for free passage. Moreover, the gas installation tubing 83 is connected to the source 84 of gas supply. And gas is supplied to the gas installation tubing 83 from the source 84 of gas supply, and gas is introduced in the processing room 82 through the gas installation tubing 83. Various kinds of gas used as the raw material of thin film formation is used for this gas, and when required, inert gas is used as carrier gas.
[0049] The flueing tubing 85 which exhausts the gas in the processing room 82 is connected to the lower part of the processing room 82, and the flueing tubing 85 is connected to the exhaust air means which consists of a vacuum pump etc. and which is not illustrated. And the gas in the processing room 82 is exhausted from the flueing tubing 85 by this exhaust air means, and the inside of the processing room 82 is set as the desired pressure.
[0050] Moreover, the installation base 87 in which Wafer W is laid is arranged at the lower part of the processing room 82.
[0051] With the gestalt of this operation, Wafer W is laid on the installation base 87 by the electrostatic chuck which Wafer W and ****** size do not illustrate. The heat-source means which is not illustrated is installed inside this installation base 87, and it is formed in the structure where the processing side of the wafer W laid on the installation base 87 can be adjusted to desired temperature.
[0052] The magnitude of this installation base 87 is the magnitude which can lay the 300mm major-diameter wafer W, and has become the device in which the wafer W laid if needed can be rotated.
[0053] Thus, by building in the large-sized installation base 87, the 300mm major-

diameter wafer W can be processed, and the high yield and the cheap manufacturing cost brought about as a result can be realized.

[0054] Opening 82a for taking Wafer W in and out of processing room 82 wall surfaces on the right-hand side of the installation base 87 is prepared among drawing 5 , and closing motion of this opening 82a is performed by moving a gate valve 98 to drawing Nakagami down. Among drawing 5 R> 5, further, proximal [of the conveyance arm (illustration abbreviation) of a gate valve 98 which conveys Wafer W in right-hand side] is carried out, it goes in and out in the processing room 82 through opening 82a, and Wafer W is laid on the installation base 87, or a conveyance arm takes out the wafer W after processing from the processing room 82. Above the installation base 87, the shower head 88 as a shower member is arranged. This shower head 88 is formed so that the space between the installation base 87 and the gas installation tubing 83 may be divided, for example, it is made from aluminum etc.

[0055] The shower head 88 is formed so that gas outlet 83a of the gas installation tubing 83 may be located in the center of the upper part, and it is introduced in the shower head 88 with which the gas introduced in the processing room 82 was arranged in the processing room 82 as it was.

[0056] Next, how to form the insulator layer which consists of gate dielectric film 2 on Wafer W is explained using above-mentioned equipment.

[0057] Drawing 6 is the flow chart which showed the flow of each process of the approach of this invention.

[0058] First, field oxide 11 is formed in a wafer W front face at the process of the preceding paragraph.

[0059] Subsequently, the wafer W with which the gate valve (illustration abbreviation) prepared in the side attachment wall of a vacuum housing 50 was opened, and field oxide 11 was formed in said silicon substrate 1 front face of the conveyance arms 37 and 38 is laid on the installation base 52.

[0060] Then, after closing a gate valve and sealing the interior, an internal ambient atmosphere is exhausted through an exhaust pipe 53 with a vacuum pump 55, vacuum suction is carried out to a predetermined degree of vacuum, and it maintains to a predetermined pressure. On the other hand, it is 2.45GHz (3kW microwave is generated, this microwave is guided from waveguide 51 **, it introduces in a vacuum housing 50 through RLSA60 and the gas supply room 54, and, thereby, the RF plasma is generated in the plasma field P by the side of the upper part in a vacuum housing 50.) from the microwave power supply section 56.

[0061] Microwave is transmitted in the condition that the inside of rectangular waveguide 63D was transmitted in rectangle mode, it was changed into the circular mode from rectangle mode in coaxial guided wave converter 63C, cylindrical shape coaxial waveguide 63B was transmitted in the circular mode, and it was able to extend in circular-waveguide 63A further, is emitted from slot 60a of RLSA60, penetrates the gas supply room 54, and is introduced into a vacuum housing 50 here. Under the present circumstances, since the plasma of high density occurs since microwave is used, and microwave is emitted from much slot 60a of RLSA60, the plasma will become high-density.

[0062] And Xe gas which is the 1st gas from a gas supply line 72 while adjusting the temperature of the installation base 52 and heating Wafer W at 400 degrees C and N2 Gas and H2 Gas and O2 Gas is introduced by the flow rate of 500sccm(s), 25sccm, 15sccm, and 1.0sccm, respectively, and the 1st process is carried out.

[0063] At this process, as the plasma style generated in the vacuum housing 3 is activated (plasma-izing) and this plasma shows the introduced gas to drawing 7 (a), the acid nitriding of the front face of a silicon substrate 1 is carried out, and the 1st insulator layer (SiON film) 21 is formed. In this way, this nitriding treatment is performed, for example for 30 seconds, and the 1st insulator layer (SiON film) 21 with a thickness of 1nm is formed.

[0064] Next, open a gate valve, the conveyance arms 37 and 38 are made to advance

into a vacuum housing 50, and the wafer W on the installation base 52 is received. After the conveyance arms 37 and 38 take out Wafer W from the plasma treatment unit 32, they are set to the installation base 87 in the adjoining CVD processing unit 33.
[0065] Subsequently, CVD processing is performed on Wafer W within this CVD processing unit 33, and the 2nd insulator layer is formed on the 1st insulator layer formed previously.
[0066] 400 degrees C and a process pressure within a vacuum housing 3 namely, for example, in the state of 50mTorr(s) - 1Torr [wafer temperature] (The gas 4, for example, SiH, which contains Si from .84 of gas supply, i.e., a source, which introduces the 2nd gas in a container 82 and carries out the 2nd process While introducing gas by the flow rate of for example, 15sccm(s)) It is Xe gas and N2 from the gas installation tubing 83. Gas is introduced by the flow rate of 500sccm(s) and 20sccm, respectively.
[0067] At this process, the 2nd introduced gas is deposited on Wafer W, and thickness increases comparatively for a short time. As shown in drawing 7 (b) in this way, the 2nd insulator layer (SiN film) 22 is formed in the front face of the 1st insulator layer (SiON film) 21. Since a membrane formation rate is a part for 4nm/, this SiN film 22 performs this membrane formation processing, for example for 30 seconds, and forms the 2nd insulator layer (SiN film) 22 with a thickness of 2nm. Thus, gate dielectric film 2 with a thickness of 4nm is formed in [.total] 30 seconds.
[0068] At the 1st above-mentioned process, it faces forming the 1st insulator layer. Under a raw gas ambient atmosphere By irradiating microwave through the flat antenna member (RLSA) which has two or more slits to the wafer W which uses silicon as a principal component, oxygen, Or since the plasma containing nitrogen or oxygen, and nitrogen is formed, oxidation, nitriding, or acid nitriding is directly performed to said processed base front face and the insulator layer is formed in it using this plasma, quality is high and can perform membraneous control with the sufficient result.
[0069] That is, the quality of the 1st insulator layer is high as shown in drawing 8 .
[0070] As shown in drawing 8 , it became possible to secure interface state density with low thermal oxidation film and this level, and to reduce the thrust omission of the pressure resistance of gate dielectric film, and the boron in a gate electrode by the semi-conductor manufacture approach of this invention.
[0071] On the other hand, by the SiN film by direct nitriding and the CVD method, interface state density increased compared with the thermal oxidation film. In this case, distribution of the carrier in an interface becomes large and the drive current of a transistor falls.
[0072] Thus, the reason the quality of the 1st insulator layer formed by the above-mentioned approach becomes high is considered as follows.
[0073] That is, by the semi-conductor manufacture approach of this invention, both a nitrogen atom and an oxygen atom carry out termination of the association of a silicon atom to a silicon substrate interface efficiently, and a dangling bond decreases. moreover, the pressure resistance of gate dielectric film and boron -- it receives running and the CVD-SiN film is acting effectively. Consequently, by the semi-conductor manufacture approach of this invention, the advantage of the direct acid nitriding SiON film and the CVD-SiN film can be used with the sufficient result.
[0074] On the other hand, when forming an interface only by SiN, the termination of a dangling bond is considered that were imperfect, for this reason interface state density increased.
[0075] Moreover, the 2nd insulator layer formed on said 1st insulator layer can be formed by performing the 2nd process of the above in a short time. Consequently, as shown below for forming the insulator layer 2 whole, it can finish in a short time.
[0076] For example, the RLSA plasma is used about formation of the first insulator layer SiON, and it is pressure 100mTorr, Xe and N2, H2, and O2. If a quantity of gas flow is respectively formed at 500sccm(s), 25sccm, 15sccm, and the 1sccm temperature C of 400 degrees, as shown in drawing 9 , the 1nm SiON film can be formed in about 30 seconds.

[0077] However, it needed for forming the 3nm SiON film on these conditions for 245 seconds. It is O2 at this membrane formation rate. Even if it made the flow rate into zero, it hardly changed. On the other hand, at CVD, they are Xe, SiH4, and N2. In 500sccm(s), 15sccm, 20sccm, and the temperature C of 400 degrees, the membrane formation rate of 4.5 nm/min extent was respectively attained in the quantity of gas flow. Therefore, in 2nm thickness, it is less than about 30 seconds, and was formed. Consequently, by the semi-conductor manufacture approach of this invention, it is less than about 60 seconds of totals, and since a 3nm insulator layer can be formed, compared with direct nitriding, a membrane formation rate can be raised sharply.
[0078] moreover, the thickness change by membrane formation of the direct acid nitriding by the above-mentioned RLSA plasma is shown in drawing 1 - as -- about 1nm ***** -- time amount -- it is proportional -- **** -- surface reaction -- it turns out that it is rate-limiting. However, if it becomes more than this, it will become a diffusion limitation and a membrane formation rate will fall gradually. Therefore, by the semi-conductor manufacture approach of this invention, the 1nm SiON film was formed by direct acid nitriding, and the SiN film was formed with the CVD method after this.
[0079] (Example) An example is shown below.
[0080] By the semi-conductor manufacture approach of this invention, the 2nm SiON film was formed in the processing unit of 32 in drawing 2 using the RLSA plasma using equipment as shown in drawing 2 on n mold silicon substrate which performed isolation formation. The thickness of a total insulator layer is 3nm (oxide-film conversion thickness). About SiON membrane formation conditions, it is Xe/N2 / H2 / O2. Flow rate = in 500sccm/25sccm/15sccm/1sccm, the pressures were 100mTorr(s), microwave power was 2.0kW, and temperature was 400-degreeC.
[0081] About the formation conditions of the CVD-SiN film, it is Xe/SiH4 / N2. Flow rate = the pressure was [the temperature of 100mTorr(s) and microwave] 400-degreeC in 25kW at 500sccm/15sccm/20sccm. Membrane formation time amount was 62 seconds, and the throughput attained h in 40 sheets /, and it has checked that it was industrially applicable enough level.
[0082] The result also with the homogeneity of thickness as good at three sigmas as 3% was obtained.
[0083] Succeedingly, the p mold poly-Si-gate was formed in gate-dielectric-film formation, and a gate leakage current and interface state density were measured to it. Consequently, gate leakage obtained the result with as good 1.3x10-6 A/cm2 and interface state density as 6.5x1010-/cm2 / eV to the impression electric field of 75 mV/cm. Furthermore, when p-MOSFET (L/W=0.25 / 10 micrometers) was formed and the ON state current was measured, the oxide film and the value more than comparable (5.5x10-4A/micrometer) were acquired.
[0084] As shown above, about 3nm good gate dielectric film was able to be industrially formed at sufficient membrane formation rate by the semi-conductor manufacture approach of this invention.
[0085]
[Effect of the Invention] Since according to this invention the direct plasma is supplied on a silicon substrate by the approach using the so-called RLSA antenna of irradiating microwave through the flat antenna member which has two or more slits and a SiN insulator layer is formed in the processed base which uses silicon as a principal component under a raw gas ambient atmosphere, membraneous control of the interface of a silicon substrate and the SiN insulator layer formed in the front face can be performed with the sufficient result.
[0086] Furthermore, according to other semi-conductor manufacture approaches of this invention, since the 1st insulator layer was formed upwards by the approach using the so-called RLSA antenna and the 2nd insulator layer is formed, the SiN film of high quality can be formed. When forming especially the 2nd insulator layer with a CVD method, film production in a short time is attained, and the SiN film of high quality can be formed in a short time.